# Reliability-Constrained Processor Performance Optimization via Design Parameter Selection

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Current high-performance processors suffer from soft error susceptibility issues which are generated in twofold aspects. The electronic noises, which usually come from large power supplies, strong radiation, or high-energy particle strikes [3], may invert some logic bits of processor structures, introducing transient faults (or equally soft errors) into the system. On the other hand, there is a strong decreasing tendency in the development of processor feature size and supply voltage, but the clock frequency and on-chip transistor density are fast increasing. These factors make current processors extremely vulnerable to soft errors. The efficient soft error rate (SER) is the product of raw SER and the probability that a soft error produces a visible error in the program output. The former is determined by the circuit properties, e.g. the critical charge of a cell, while the latter is characterized at microarchitectural level by the Architectural Vulnerability Factor (AVF) [2], which is proposed based on the observation that a large amount of raw soft errors are masked at the architectural level. A common approach to calculate a processor structure's AVF is via Architecturally Correct Execution (ACE) analysis [2]: count the number of bits that are required for correct execution, and then divide it by the total number of bits of the structure. Therefore, the AVF is usually used to estimate processor soft error robustness.

In this work, we propose reliable and high performance processor design parameter selection at the pre-silicon stage. We analyze the design choices optimized for performance, reliability to soft errors and their tradeoff, respectively, by exploring a large design space consisting of several key configuration parameters for both single-core and multi-core processors.

We propose using two techniques to configure design parameters to optimize processor performance under reliability constraints. Given a few sampled simulation results, we characterize the design space using *Patient Rule Induction Method* (PRIM) [1] to generate a set of selective rules on key design parameters. Applying these rules on the design space effectively identifies the configurations that achieve the optimization for a certain metric, e.g. the AVF. This technique provides computer architects with useful guidelines to design reliable processors while achieving high performance. The other approach proposed in this paper to select desired configurations for different optimizations is heuristic pareto frontier analysis with reduced design space, namely *Subspace Pareto Frontier Identification* (SPFI). Basically, a predictive model is trained using a subset of parameters which turn out to be important to the response. We only perform predictions for the points in a significantly reduced design space to identify the performance optima under different vulnerability constraints. This mechanism avoids exhaustively evaluating the original large design space, thereby reducing large prediction overheads.

In summary, the main contributions of this paper are as follows:

- **Reliable processor design parameter selection**: We are capable of extracting a certain region of the design space by applying a set of selective rules on the parameters. The identified design space region is towards the optimization of the AVF, so the rules generated are guidelines for achieving reliable single and multi-core processor design.
- **Optimizing holistic reliability**: We quantitatively show that reducing the AVF of a single structure may increase the vulnerability of other parts of the core. Similarly, reducing the AVF of one core may also affect another core's AVF. This addresses the demand for a holistic reliability optimization. Our method can also generate rules for global reliability optimization, especially for shared resource of multi-core processors.
- **Balancing reliability and performance**: We quantitatively demonstrate that, for some individual structures and the entire processor, merely minimizing their vulnerability significantly degrades performance. Simultaneously optimizing performance and reliability tends to mitigate the imbalance.
- **Heuristic reliability-constrained performance optima identification**: By selecting a few important design variables, we construct a new small design space for evaluation, thus avoiding exhaustively predicting the original large design space. The experimental results demonstrate the accuracy of our method.

## References

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